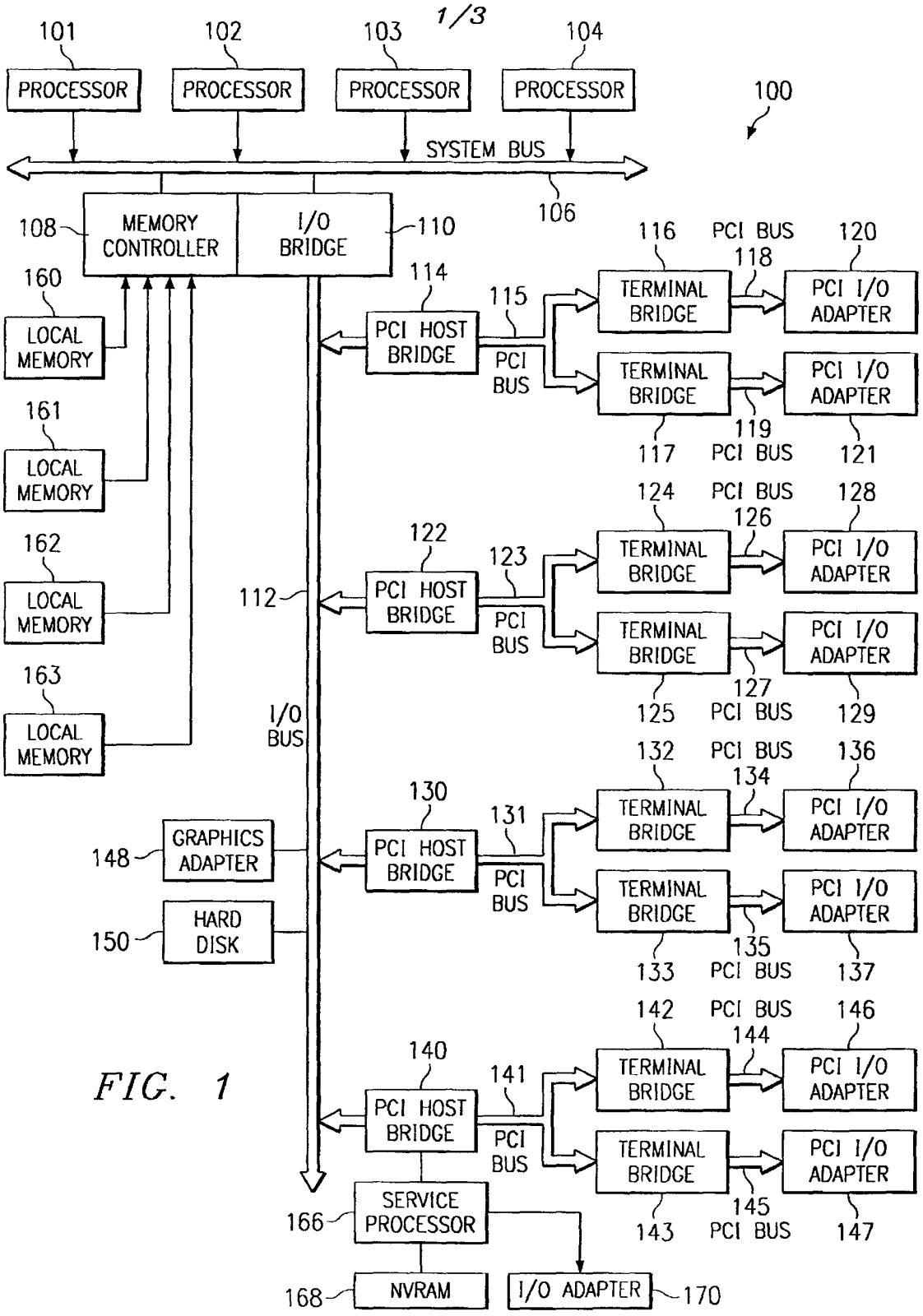

101
102
103
104
PROCESSOR
PROCESSOR
PROCESSOR
PROCESSOR
100
SYSTEM BUS
106
108
MEMORY CONTROLLER
I/O BRIDGE
110
160
LOCAL MEMORY
161
LOCAL MEMORY
162
LOCAL MEMORY
163
LOCAL MEMORY
112
I/O BUS
114
PCI HOST BRIDGE
115
PCI BUS
116
PCI BUS
118
TERMINAL BRIDGE
120
PCI I/O ADAPTER
TERMINAL BRIDGE
PCI I/O ADAPTER
117
119
PCI BUS
121
122
PCI HOST BRIDGE
123
PCI BUS
124
PCI BUS
126
TERMINAL BRIDGE
128
PCI I/O ADAPTER
TERMINAL BRIDGE
PCI I/O ADAPTER
125
127
PCI BUS
129
130
PCI HOST BRIDGE
131
PCI BUS
132
PCI BUS
134
TERMINAL BRIDGE
136
PCI I/O ADAPTER
TERMINAL BRIDGE
PCI I/O ADAPTER
133
135
PCI BUS
137
148
GRAPHICS ADAPTER
150
HARD DISK
140
PCI HOST BRIDGE
141
PCI BUS
142
PCI BUS
144
TERMINAL BRIDGE
146
PCI I/O ADAPTER
TERMINAL BRIDGE
PCI I/O ADAPTER
143
145
PCI BUS
147
166
SERVICE PROCESSOR
168
NVRAM
I/O ADAPTER
170

FIG. 1

212
RUN TIME SYSTEM FIRMWARE
PROCESSOR
210
HARDWARE LOGIC
200
202
L1 CACHE AND TAG
ERAT
204
TLB
206
208
SRR1 AND DSISR REGISTERS

FIG. 2

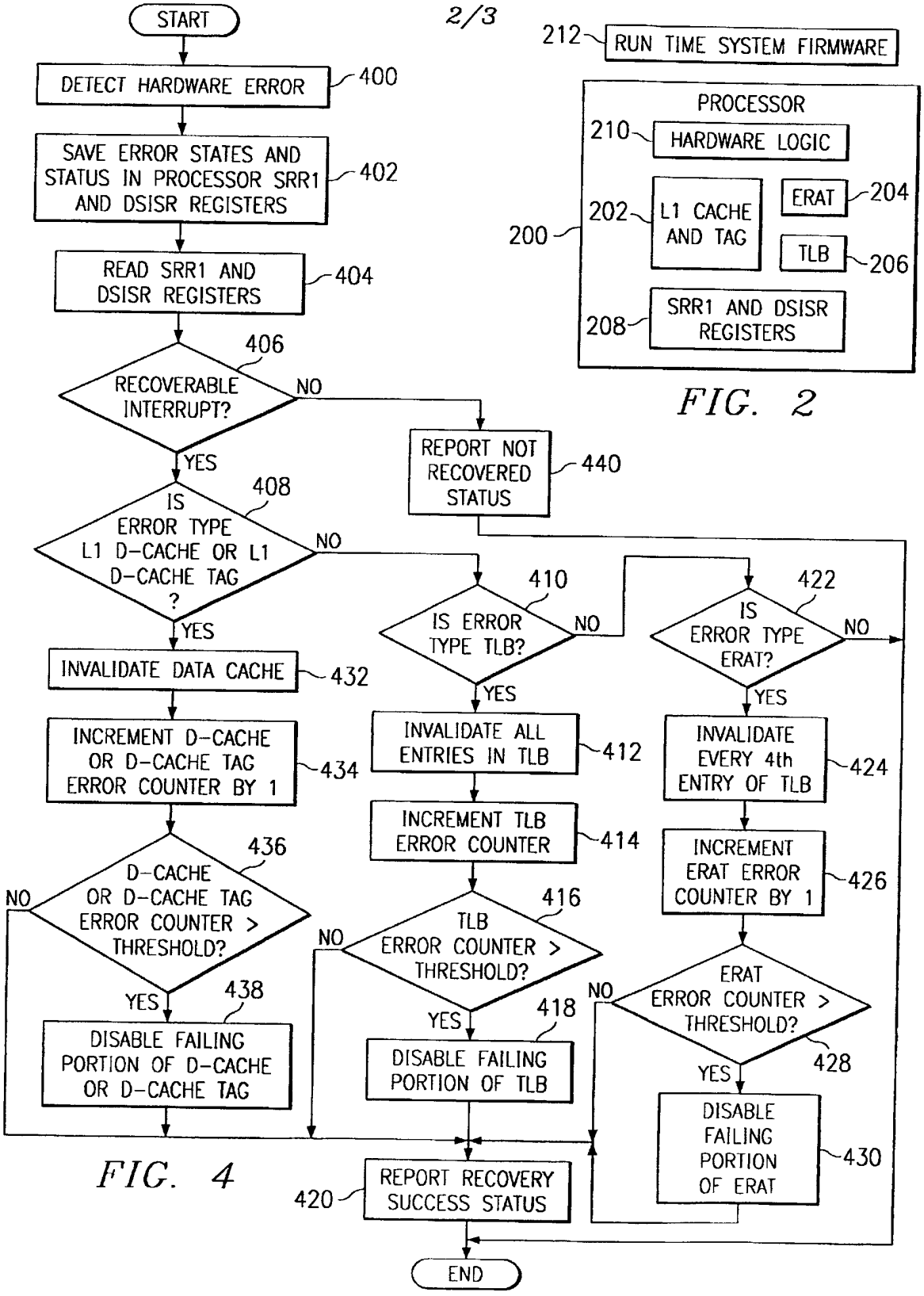
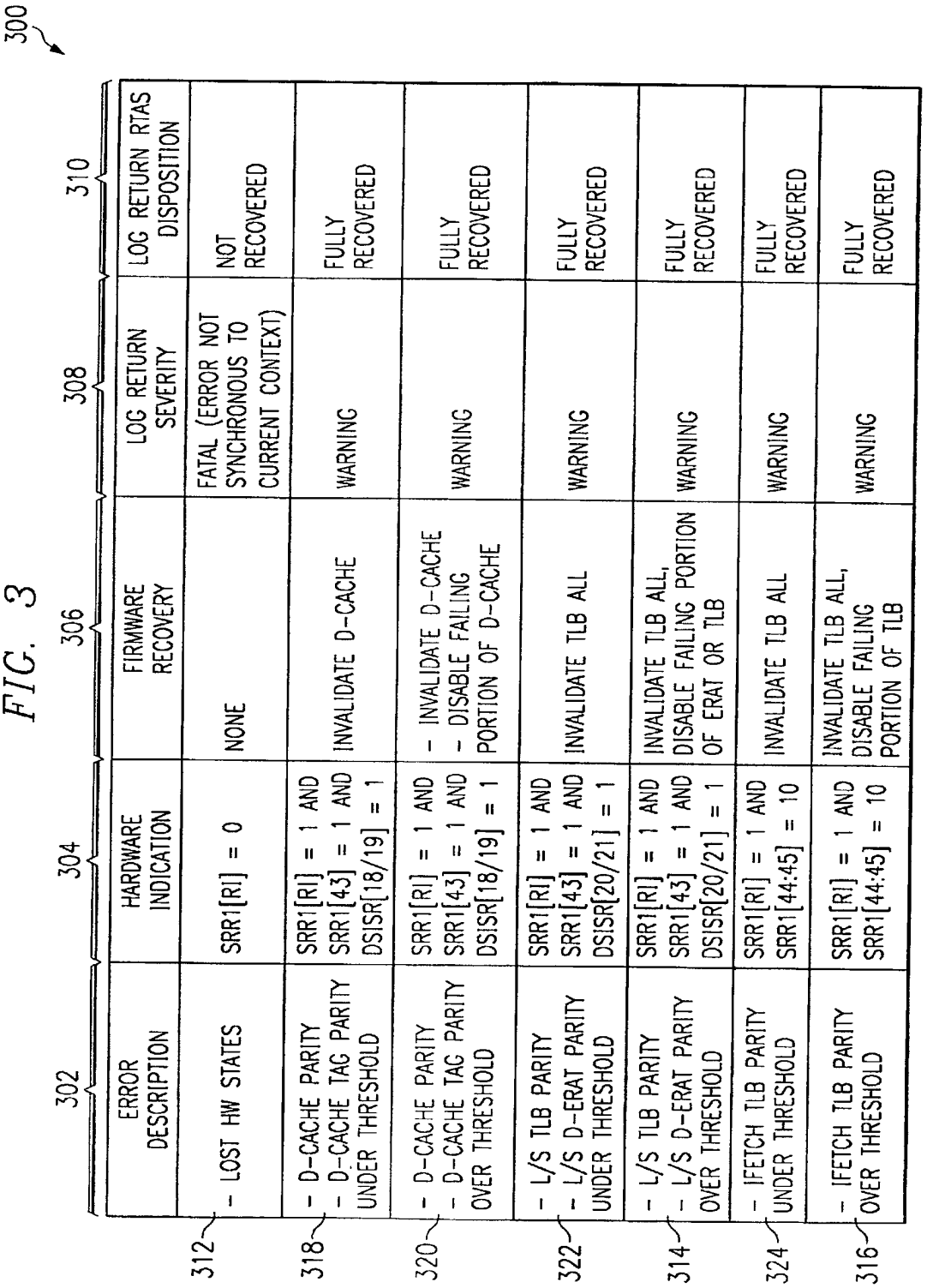

START
DETECT HARDWARE ERROR
400
SAVE ERROR STATES AND STATUS IN PROCESSOR SRR1 AND DSISR REGISTERS
402
READ SRR1 AND DSISR REGISTERS
404
406
RECOVERABLE INTERRUPT?
NO
YES
REPORT NOT RECOVERED STATUS
440
408
IS ERROR TYPE L1 D-CACHE OR L1 D-CACHE TAG ?
NO
YES
INVALIDATE DATA CACHE
432
INCREMENT D-CACHE OR D-CACHE TAG ERROR COUNTER BY 1
434
436
D-CACHE OR D-CACHE TAG ERROR COUNTER > THRESHOLD?
NO
YES
438
DISABLE FAILING PORTION OF D-CACHE OR D-CACHE TAG
410
IS ERROR TYPE TLB?
NO
YES
INVALIDATE ALL ENTRIES IN TLB
412
INCREMENT TLB ERROR COUNTER
414
416
TLB ERROR COUNTER > THRESHOLD?
NO
YES
418
DISABLE FAILING PORTION OF TLB
422
IS ERROR TYPE ERAT?
NO
YES
INVALIDATE EVERY 4th ENTRY OF TLB
424
INCREMENT ERAT ERROR COUNTER BY 1
426
ERAT ERROR COUNTER > THRESHOLD?
428
NO
YES
DISABLE FAILING PORTION OF ERAT
430
REPORT RECOVERY SUCCESS STATUS
420
END

FIG. 4

FIG. 3



ERROR DESCRIPTION	HARDWARE INDICATION	FIRMWARE RECOVERY	LOG RETURN SEVERITY	LOG RETURN RTAS DISPOSITION
- LOST HW STATES	SRR1[RI] = 0	NONE	FATAL (ERROR NOT SYNCHRONOUS TO CURRENT CONTEXT)	NOT RECOVERED
- D-CACHE PARITY - D-CACHE TAG PARITY UNDER THRESHOLD	SRR1[RI] = 1 AND SRR1[43] = 1 AND DSISR[18/19] = 1	INVALIDATE D-CACHE	WARNING	FULLY RECOVERED
- D-CACHE PARITY - D-CACHE TAG PARITY OVER THRESHOLD	SRR1[RI] = 1 AND SRR1[43] = 1 AND DSISR[18/19] = 1	- INVALIDATE D-CACHE - DISABLE FAILING PORTION OF D-CACHE	WARNING	FULLY RECOVERED
- L/S TLB PARITY - L/S D-ERAT PARITY UNDER THRESHOLD	SRR1[RI] = 1 AND SRR1[43] = 1 AND DSISR[20/21] = 1	INVALIDATE TLB ALL	WARNING	FULLY RECOVERED
- L/S TLB PARITY - L/S D-ERAT PARITY OVER THRESHOLD	SRR1[RI] = 1 AND SRR1[43] = 1 AND DSISR[20/21] = 1	INVALIDATE TLB ALL, DISABLE FAILING PORTION OF ERAT OR TLB	WARNING	FULLY RECOVERED
- IFETCH TLB PARITY UNDER THRESHOLD	SRR1[RI] = 1 AND SRR1[44:45] = 10	INVALIDATE TLB ALL	WARNING	FULLY RECOVERED
- IFETCH TLB PARITY OVER THRESHOLD	SRR1[RI] = 1 AND SRR1[44:45] = 10	INVALIDATE TLB ALL, DISABLE FAILING PORTION OF TLB	WARNING	FULLY RECOVERED